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(Embodiments)

Referring to the attached drawings, the following describes a driving method of a liquid crystal display device in one embodiment of the present invention.

Fig. 1 schematically shows a liquid crystal display device (1) of the present embodiment, based on which a driving method of a liquid crystal display device of the present invention is realized. The liquid crystal display device (1) includes 640 signal electrodes X_i ($i = 1, 2, \dots, 640$) (11) connected to a signal electrode driving circuit (101), and 480 scanning electrodes Y_j ($j = 1, 2, \dots, 480$) (21) connected to a scanning electrode driving circuit (201). The signal electrodes X_i and the scanning electrodes Y_j are disposed in a matrix, and a pixel electrode (41) connected to a thin film transistor (31) is disposed at each intersection of the signal electrodes X_i and the scanning electrodes Y_j .

A plurality of pixel electrodes (41) connected to a single scanning electrode Y_j (21) make up a scanning line P_j ($j = 1, 2, \dots, 480$) (not shown).

Page 2**Japanese Patent No. 2585463**

In the thin film transistor (31), a gate electrode (31a) is connected to the scanning electrode Yj (21), a source electrode (31b) is connected to the signal electrode Xi (11), and a drain electrode (31c) is connected to the pixel electrode (41), wherein ON/OFF control of the source electrode (31b) and the drain electrode (31c) is carried out according to a gate pulse GP supplied to the gate electrode (31a) from the scanning electrode driving circuit (201). Between the pixel electrode (41) and a counter electrode (51) corresponding thereto is interposed a liquid crystal composition (61), wherein the liquid crystal display device (1) has black display when the potential difference between the pixel electrode (41) and the counter electrode (61) is 0V.

A second display mode of the liquid crystal display device (1) is described below in which 400 among 480 scanning lines Pj ($j = 1, 2, \dots, 480$) (22) are effective scanning lines Pj ($j = 1, 2, \dots, 400$) that make up a display region (24), as illustrated in Fig. 2.

The signal electrode driving circuit (101) receives a video signal SIG that includes a display signal (83) and a non-display signal (81) shown in Fig. 3, and per one scanning period, the signal electrode driving circuit (101) sequentially outputs a video signal SIG of one scanning line Pj (22) to the respective signal electrodes Xi (11). The scanning electrode driving circuit (201) sequentially applies a gate pulse GP shown in Fig. 3 to the respective

Page 3**Japanese Patent No. 2585463**

scanning electrodes Y_j (21) per one scanning period.

In this manner, the effective scanning lines P_j are sequentially scanned within a display period T_d , thereby displaying a display signal in the display region (24).

Within a retrace period T_b , the scanning lines P_j ($j = 401, 402, \dots, 480$) in the non-display region (25) are scanned at once, thus obtaining black display in the non-display region (25).

In this manner, all the scanning lines P_j ($j = 1, 2, \dots, 480$) (22) are scanned within one field period T_f to carry out display.

The following describes a specific structure of the scanning electrode driving circuit (201) for generating a gate pulse GP.

Fig. 4 illustrates an equivalent circuit of a main portion of the main scanning electrode driving circuit (201), the circuit including shift registers with a set-reset function as realized by 480 D flip-flops $D1_j$ (203) ($j = 1, 2, \dots, 480$) that are connected so that a scanning start signal ST from an ST signal terminal (213) is sequentially transferred according to a clock signal CK from a CK signal terminal.

The D flip-flop $D1_j$ (203) is connected so that the output therefrom is applied as a gate pulse GP to a respective scanning electrode Y_j (21) after it is controlled

Page 4**Japanese Patent No. 2585463**

to a predetermined voltage by a level shifter 209. Further, to the D flip-flop D1j (203) is connected the output of an AND gate (207) for carrying out set-reset control for the D flip-flop D1j (203). One of the input terminals of the AND gate (207) is connected to a SET signal terminal (215), and the other input terminal is connected to the output of a D flip-flop D2j (205) ($j = 1, 2, \dots, 480$) that operates using the output of the D flip-flop D1j (203) as a clock. The scanning electrode driving circuit (201) is so structured.

The foregoing display operation is realized by applying a shift clock signal CK, a scanning start signal ST, a set signal SET, and a clear signal CLR as shown in Fig. 3 to the CK signal terminal (211), the ST signal terminal (213), the SET signal terminal (215), and the CLR signal terminal (217), respectively, of the scanning electrode driving circuit (201) having the foregoing circuit structure.

That is, the scanning start signal ST is sequentially transferred to the D flip-flops D1j (203) according to the shift clock signal CK, and is outputted as a gate pulse GP to each scanning electrode Yj (21). In this manner, all the effective scanning lines Pj ($j = 1, 2, \dots, 400$) are scanned within a display period Td, thus displaying information.

When the selection of the 400th scanning electrode Yj (21) is finished, the 401st to 480th scanning electrodes

Page 5**Japanese Patent No. 2585463**

Yj (21), i.e., only the scanning electrodes Yj (21) in the non-display region (26) become settable by the set signal SET supplied from the SET signal terminal (215). As a result, the set signal ST transferred with the next shift clock signal CK is outputted as a gate pulse GP of a predetermined voltage from the level shifter (209) to each of the 401st to 480th scanning electrodes Yj (21). In this manner, the non-display signal (81) (see Fig. 3) is applied at once to the scanning lines Pj of the non-display region (35) within a retrace period Tb.

The clear signal CLR resets all the D flip-flops Dlj (203) to enable the next display.

As described, with the driving method of the liquid crystal display device of the present embodiment, driving of the effective scanning lines Pj, which are smaller in number than the entire scanning lines Pj (22), can also be carried out with a simple circuit structure and without reducing the time axis, by applying the non-display signal (81) at once to the scanning lines Pj (22) in the non-display region (25) within a retrace period Tb.

The following describes a driving method of a liquid crystal display device in another embodiment of the present invention.

Fig. 5 shows a display screen in a second display mode, in which 400 effective scanning lines Pj ($j = 41, 42,$

Page 6**Japanese Patent No. 2585463**

..., 440) make up a display region (24), and non-display regions (23) and (25) each having 40 scanning lines P_j are provided above and below the display region (24), respectively.

Such display can readily be realized by selecting each scanning electrode Y_j (21) by the gate pulse GP for example shown in Fig. 6, and by applying a video signal SIG.

In the video signal SIG shown in Fig. 6, one frame period T_f includes a display period T_d and a retrace period T_b , wherein the display period T_d includes a display signal (83) and a non-display signal (81).

The gate pulse GP shown in Fig. 6 is sequentially supplied to the scanning electrode Y_i (21) per one scanning period, and display information is displayed by the effective scanning lines P_j ($j = 41, 42, \dots, 440$).

Within the retrace period T_b in one frame period T_f , the gate pulse GP shown in Fig. 6 at once scans the scanning lines P_j ($j = 1, 2, \dots, 40$), P_j ($j = 441, \dots, 480$) other than the effective scanning lines P_j ($j = 41, 42, \dots, 440$), and the non-display signal (81) is applied. In this manner, all the scanning lines P_j (22) are scanned within one frame period to realize one display.

Referring to the equivalent circuit diagram of a scanning electrode driving circuit (301) illustrated in Fig.

Page 7**Japanese Patent No. 2585463**

7, the following describes one embodiment of the scanning electrode driving circuit (201) of the liquid crystal display device (1) realizing the foregoing driving.

D flip-flops D1j ($j = 1, 2, \dots, 480$) (303) constitute shift registers. A first-stage D flip-flop D11 (303) receives an input signal D13 from an input terminal (317), and the input signal D13 is sequentially transferred with a shift clock CK2 supplied from the input terminal (319).

The output terminal Q of each flip-flop D1j (303) is the input of the next-stage D flip-flop D1j (303), and is connected to a switching element S1 (305) so as to control switching elements S_j ($j = 1, 2, \dots, 480$) (305) for selecting one of two inputs. One of the input terminals of a first-stage switching element S1 (305) receives a signal D11 from the input terminal (311), and the other switching elements S_j (305) each has an input terminal that is connected to the output terminal Q of the D flip-flop D2j ($j = 1, 2, \dots, 479$) (307). Further, the switching elements S_j (305) each have an input terminal that receives a signal D12 from the input terminal (315).

The D flip-flops D2j (307) each has an input terminal D that is connected to the output terminal of an adjacent one of the switching elements S_j (305), and to a respective scanning electrode Y_j (21) via a buffer BF_j ($j = 1, 2, \dots, 480$) (309). The scanning electrode driving circuit (201) is

Page 8**Japanese Patent No. 2585463**

so structured.

By supplying a predetermined signal DI3 to the input terminal (317), the switching elements S_j ($j = 1, \dots, 40$), S_j ($j = 441, \dots, 480$) (305) are controlled to select the input signal DI2 from the input terminal (315), and the switching elements S_j ($j = 41, \dots, 440$) (305) are controlled to be connected to the output terminals Q of the S flip-flops D2j ($j = 40, \dots, 439$) (207), enabling the gate pulse GP as shown in Fig. 6 to be easily outputted.

The foregoing described the display mode (see Fig. 5) in which display is carried out with 400 effective scanning lines, among which scanning lines P_j ($j = 41, \dots, 440$) make up the display region (24), and scanning lines P_j ($j = 1, \dots, 40$), P_j ($j = 441, \dots, 480$) make up the non-display regions (23) and (25). However, display modes with different numbers of effective scanning lines P_j may be accommodated according to the signal DI13 supplied to the input terminal (217).

Further, according to the signal DI3 supplied to the input terminal (217), a display position can readily be changed.

Referring to the drawings, another embodiment of the present invention is described below.

As in the foregoing embodiment, description is made as to the second display mode in which 400 of 480

Page 9**Japanese Patent No. 2585463**

scanning lines P_j are the effective scanning lines P_j , as shown in Fig. 5.

Fig. 8 is a timing chart showing one example of a driving method of a liquid crystal display device of the present embodiment. In the driving method of the liquid crystal display device (1) of the present embodiment, the effective scanning lines P_j ($j = 41, 42, \dots, 440$) are sequentially scanned per one frame period to apply a display signal (83), and then, within a retrace period T_b in one frame period T_f , the scanning lines P_j ($j = 1, \dots, 40$) and the scanning lines P_j ($j = 441, \dots, 480$) other than the effective scanning lines P_j ($j = 41, 42, \dots, 440$) are scanned to apply a non-display signal (81a) and a non-display signal (81b), respectively.

In this manner, in the second display mode in which the effective scanning lines P_j are smaller in number than all the scanning lines P_j , the scanning lines P_j other than the effective scanning lines P_j may be divided into two groups within a retrace period T_b to apply the non-display signals (81a) and (81b).

In this way, display can easily be carried out, as in the foregoing embodiment, for different numbers of effective scanning lines, without providing a memory element such as frame memory, or time axis changing means, etc., in the liquid crystal display device (1).

Page 10**Japanese Patent No. 2585463**

Referring to the equivalent circuit diagram of a scanning electrode driving circuit shown in Fig. 9, the following describes one example of a scanning electrode driving circuit (401) of the liquid crystal display device (1) that realizes the foregoing driving.

In Fig. 9, switching elements $S1j$ ($j = 1, 2, \dots, 480$) (405) are controlled by the outputs of a serial-parallel conversion circuit (403). A first-stage switching element $S11$ (405) is connected to three input terminals (421), (425), (427) to select between inputs $DI1$, $DI2$, and $DI3$.

The other switching elements $S1j$ ($j = 2, \dots, 480$) (405) are respectively connected to outputs Q of D flip-flops Dj ($j = 1, 2, \dots, 479$) (407), instead of the input terminal (421).

The output Q of the D flip-flop Dj (407) is connected to each scanning electrode Yj (21) via an output buffer BFj ($j = 1, 2, \dots, 480$), and becomes the input of the next-stage switching element $S1j$ ($j = 1, 2, \dots, 480$) (411) via the switching element $S2j$ ($j = 1, 2, \dots, 480$). As are the switching elements $S1j$ ($j = 2, \dots, 480$) (405), the switching elements $S2j$ (411) are ON/OFF controlled by the outputs of the serial-parallel conversion circuit (403).

By supplying a predetermined signal to the serial-parallel conversion circuit (403) of the scanning electrode driving circuit (401) having the foregoing

Page 11**Japanese Patent No. 2585463**

structure, the switching elements $S1j$ ($j = 1, 2, \dots, 40$) (405) are connected to the input $DI3$, the switching elements $S1j$ ($j = 41, 42, \dots, 440$) (405) are connected to the outputs Q of the D flip-flops Dj ($j = 40, 41, \dots, 439$) (407), and the switching elements $S1j$ ($j = 441, 442, \dots, 480$) (405) are connected to the input $DI2$. In addition, only the switch $S2j$ ($j = 440$) (411) is being connected.

As a result, the gate pulse GP is applied at once to the scanning electrodes Yj (21), and the non-display signal ($B1b$) is applied at once to the scanning lines Pj ($j = 1, 2, \dots, 40$). The gate pulse GP is sequentially applied per one scanning period to the scanning electrodes Yj ($j = 41, 42, \dots, 440$) (21) constituting the effective scanning lines Pj ($j = 41, 42, \dots, 440$), thereby applying the display signal (83) to realize one display. Further, within a retrace period Tb , the scanning lines Pj ($j = 441, 442, \dots, 480$) are scanned at once to apply the non-display signal (81a) to the non-display region (25).

With the scanning electrode driving circuit (401) having, for example, the foregoing structure to realize the driving method of the liquid crystal display device of the present embodiment, a display position can easily be changed by having different settings for the input signal to the serial-parallel conversion circuit (403).

As described, with the driving method of the liquid

Page 12**Japanese Patent No. 2585463**

crystal display device of the present embodiment, the scanning lines other than the effective scanning lines are scanned either at once or in a plurality of groups within a retrace period T_b in one frame period T_f , thereby scanning all the scanning lines within a retrace period T_b in one frame period T_f , without changing the time axis.

This enables the present invention to be realized with a simple circuit structure.